## General Description of Silicon Wafers, Substrates and Sample Supports

Polished silicon is an excellent substrate for imaging, experiments and microfabrication applications. It is available in the form of wafers, diced wafer or as smaller chips (pieces). The silicon wafer and chips all have a {100} orientation. Cleaving of the wafers to the desired size with a {100} orientation wafers is straight forward and simple. The silicon wafers and chips are all P-type, doped with B to provide excellent conductivity for SEM, FIB and STM applications. For biological applications silicon resembles glass, which makes it a suitable support for growing and/or mounting cells. For imaging applications, it is an ideal sample substrate for small particles due to the low background signal of the highly polished surface.

Two grades of silicon substrates are offered:

- Standard silicon wafers and silicon chips for standard application and medium resolution imaging.
- Ultra-flat silicon wafers and ultra-flat silicon chips for demanding applications and high resolution imaging.

To cover a wide range of applications, the silicon substrates are available as:

- Si wafers: 2”/51mm, 4”/100mm and 6”/150mm diameter
- Diced 4”/100mm wafer in 5x5mm Si chips (~270 chips)
- Ultra-flat 5x5mm Si chips;  25 packaged in a gel box
- Ultra-flat 5x5mm Si chips with 200nm thermal SiO2; 25 packaged in a gel box
- Silicon Finder Grid ultra-flat Si substrate 12.5x12.5mm. 1x1mm laser etched and numbered raster to provide unique 144 fields (equivalent with 25mesh).

### Silicon wafer, Ø2”/51mm, 275µm thickness

Silicon wafer substrate Ø2”/51mm can be used for sample substrates, micro-fabrication, substrate for thin film research or biological substrates. Useful flat substrate for SEM imaging of particles due to the low background. For biological applications, Si has similar properties as glass and can be used to mount or grow cells. Can be easily cleaved or used as a whole wafer. The Si wafer is packed in a 2”wafer carrier tray for protection.

Specifications of the Ø2”/51mm silicon wafers, 275µm thickness:

| | |
|---|---|
| Orientation | {100} |
| Type | P (Boron) with one primary flat |
| Resistance | 1-30 Ohm/cm |
| Coating | None, native oxide only |
| Thickness | 275µm (+/- 20µm) |
| Diameter | 51mm |
| TTV | =< 20µm |
| Primary Flat | 15.9 +/- 1.65mm |
| Surface roughness | <1.5nm, polished on one side |

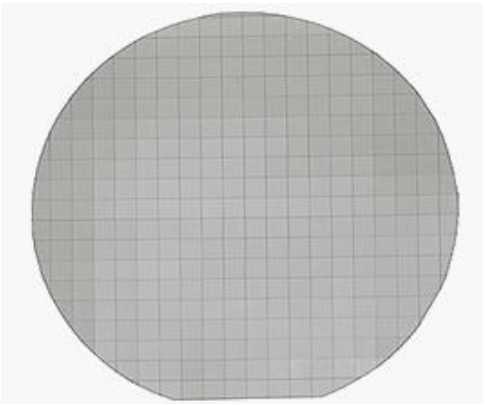
**Silicon wafer, Ø6”/150mm, 675µ thickness**

Silicon wafer substrate Ø6”/150mm can be used for sample substrates, micro-fabrication, substrate for thin film research or biological substrates. Useful flat substrate for SEM imaging of particles due to the low background. For biological applications, Si has similar properties as glass and can be used to mount or grow cells. This large wafer with the {100} orientation can be easily cleaved to the desired size. The Si wafer is packed in a 6” wafer carrier tray for protection.

Specifications of the Ø6”/150mm silicon wafers, 675µm thickness:

| | |
|---|---|
| Orientation | {100} |
| Type | P (Boron) with one primary flat |
| Resistance | 1-30 Ohm/cm |
| Coating | None, native oxide only |
| Thickness | 675µm (+/- 20µm) |
| Diameter | 150mm |
| TTV | =< 20µm |
| Primary Flat | 57.5 +/- 2.5mm |
| Surface roughness | <1.5nm, polished on one side |

**Diced silicon wafer Ø4”/100mm, 5x5mm chips, 525µm thickness**



The Ø4”/100mm silicon Wafer is diced into 5x5mm chips which is an excellent size for speciment supports. The yield for the 4”/100mm wafer is approx. 270 chips of 5x5mm. The silicon chips can be used for sample substrates, micro-fabrication, substrate for thin film research or biological substrates. Very useful flat substrate for SEM imaging of particles due to the low background. For biological applications, Si has similar properties as glass and can be used to mount or grow cells. Conveniently precut wafer chips supplied on sticky wafer dicing tape. We recommend to clean the Si chips to remove any silicon dust left after dicing or generated during transport.

Specifications of the diced Ø4”/100mm silicon wafer, 5x5mm chips, 525µm thickness:

| | |
|---|---|
| Orientation | {100} |
| Type | P (Boron) with one primary flat |
| Resistance | 1-30 Ohm/cm |

| | |
|---|---|
| Coating | None, native oxide only |
| Thickness | 525µm (+/- 20µm) |
| Chip (die) size | 5x5mm |
| Chip quantity | ~270 |
| TTV | =< 20µm |
| Primary Flat | 32.5 +/- 2.5mm |
| Surface roughness | <1.5nm, polished on one side |

**Ultra-flat P{100} silicon wafer, Ø4”/100mm, 525µm thickness**

The ultra-flat Ø4”/100mm P {100} silicon wafer has higher specifications than the standard silicon wafers. They are preferred for demanding applications in micro-fabrication, as substrates for thin film research or biological substrates. Excellent ultra-flat surface for high resolution SEM imaging of particles due to the low background signal. For biological applications, Si has similar properties as glass and can be used to mount or grow cells. This large wafer with the {100} orientation can be easily cleaved to the desired size. The Si wafer is clean-room packed in a 4” wafer carrier tray for protection.

Specifications of the ultra-flat Ø4”/100mm silicon wafers:

| | |
|---|---|
| Orientation | {100} |
| Type | P (Boron) with one primary flat |
| Resistance | 1-10 Ohm/cm |
| Grade | Prime / CZ Virgin |
| Coating | None, native oxide only |
| Thickness | 525µm (+/- 20µm) |
| Diameter | 100mm |
| Warp | =<30µm |
| Bow | =<30µm |
| Primary Flat | 32.5 +/- 2.5mm |
| Surface roughness | 02.- 0.3nm, polished one side |

**Ultra-flat P{100} silicon wafer, Ø6”/150mm, 675µm thickness**

The ultra-flat Ø6”/150mm P{100} silicon wafer has higher specifications than the standard silicon wafers. They are preferred for demanding applications in micro-fabrication, as substrates for thin film research or biological substrates. Excellent ultra-flat surface for high resolution SEM imaging of particles due to the low background signal. For biological applications, Si has similar properties as glass and can be used to mount or grow cells. This large wafer with the {100} orientation can be easily cleaved to the desired size. The Si wafer is clean-room packed in a 6”wafer carrier tray for protection.

Specifications of the ultra-flat P{100} silicon wafer, Ø6”/150mm, 675µm thickness:

| | |
|---|---|
| Orientation | {100} |
| Type | P (Boron) with one primary flat |
| Resistance | 1-10 Ohm/cm |
| Grade | Prime / CZ Virgin |
| Coating | None, native oxide only |
| Thickness | 675µm (+/- 20µm) |
| TTV | =< 1.5µm |
| Warp | =<30µm |
| Bow | =<30µm |
| Primary Flat | 57.5 +/- 2.5mm |
| Surface roughness | 02.- 0.3nm, polished one side |

**Ultra-flat P {100} silicon chips, 5x5mm, 675µm thickness**

The ultra-flat P {100} silicon wafer chips have higher specifications than the standard silicon chips. They are preferred for demanding applications in micro-fabrication, as substrate for thin film research or biological substrates. Excellent ultra-flat surface for high resolution SEM imaging of particles due to the low background signal. For biological applications, Si has similar properties as glass and can be used to mount or grow cells. The 25 ultra-flat Si wafer chips are clean-room packaged in a gel box.

Specifications of the ultra-flat P{100}silicon chips, 5x5mm, 675µm thickness:

| | |
|---|---|
| Orientation | {100} |
| Type | P (Boron) |
| Resistance | 1-10 Ohm/cm |

| | |
|---|---|
| Grade | Prime / CZ Virgin |
| Coating | None, native oxide only |
| Thickness | 675µm (+/- 20µm) |
| Chip (Die) size | 5x5mm |
| Quantity | 25 |
| TTV | =< 1.5µm |
| Warp | =<30µm |
| Bow | =<30µm |
| Surface roughness | 02.- 0.3nm, polished one side |

**Ultra-flat thermal oxide substrate on P{100}silicon chips, 5x5mm, 675µm thickness**

The, ultra-flat SiO2 substrate is a thermally grown amorphous silicon dioxide layer on ultra-flat silicon wafer chips. SiO2 is one the best characterized materials and is used in a variety of applications in life science research (cells), thin film research and semiconductor research. Excellent ultra-flat substrate for high resolution SEM or AFM imaging. To ensure debris free substrates, the wafer is coated with photo resist before dicing. The photo resist is subsequently removed in a special cleaning cycle. The 25 ultra-flat SiO2 substrates on Si wafer chips are clean-room packaged in a gel box.

Specifications of the ultra-flat thermal oxide substrate on P {100} silicon chips, 5x5mm, 675µm thickness:

| | |
|---|---|
| rientation | {100} |
| Type | P (Boron) |
| Resisantance | 1-10 Ohm/cm |
| Grade | Prime / CZ Virgin |
| Coating | 200nm thermally grown amorphous SiO2 |
| Thickness | 675µm (+/- 20µm) |
| Chip (Die) size | 5x5mm |
| Quantity | 25 |
| TTV | =< 1.5µm |

| | |
|---|---|
| Warp | =<38µm |
| Bow | =<38µm |
| Surface roughness | 02.- 0.3nm, polished one side |

**Silicon Finder Grid Substrate FG1 with 144 fields of 1x1mm**

The silicon finder grid substrate is an ultra-flat substrate with a chrome deposited raster with a 1mm pitch. This divides the substrate into 144 indexed fields of 1x1mm where each of the fields has a unique alphanumeric label in the lower right corner. The alphanumeric label is easy to see with a magnifier, stereo microscope and/or SEM. The raster produced is comparable with 25 mesh and is practical for larger particles or small samples mounted on the substrate in separate fields. The Nano-Tec FG1 silicon finder grid substrate is ideal for correlative microscopy since the locations of th e sample can be easily found again. Size of the FG1 is 12x12mm on a 12.5 x 12.5mm die.

This product has a number of advantages over engraved SEM stubs and the usual copper SEM finder grids:

- Ultra-flat – no height differences such as with copper finder grids
- Pattern is visible with unaided eye, SEM and light microscope
- Each individual field indexed with an alphanumeric label
- Low background signal for SEM imaging – similar to Si chips
- Fine pattern over entire area – finer than engraved stubs
- Sample size can be easily judged with the 1x1mm pattern in the background
- Easy to mount on SEM and AFM stubs
- Compatible with SEM, FIB, AFM, LM, XPS/ESCA, SIMS and Auge

The silicon finder grid substrate FG1 is packaged in a clean-room and shipped in a gel box.

Specifications of the Silicon Finder Grid Substrate with 144 fields of 1x1mm:

| | |
|---|---|
| Pattern size | 12 x12 mm divided into 144 1x1mm fileds |
| Pattern/labels | 75nm thick deposited Cr with 20µm line width, 80µm label height |
| Die size | 12.5x12.5mm |
| Orientation | {100} |
| Type | P (Boron) |
| Resisantance | 1-10 Ohm/cm |
| Grade | Prime / CZ Virgin |

| | |
|---|---|
| Coating | None, native oxide only |
| Thickness | 675µm (+/- 20µm) |
| TTV | =< 1.5µm |
| Warp | =<30µm |
| Bow | =<30µm |
| Surface roughness | 02.- 0.3nm, polished one side |